

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Nobuyoshi Tsukaguchi et al.  
Serial No. : 10/713,390  
Filed : November 14, 2003  
Confirmation No:  
TC/A.U. :  
Examiner :

Docket No. : 02-668-US-2  
Customer No. : 34704

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

In accordance with the requirements of 37 CFR 1.97 and 1.98, Applicant hereby submits the documents listed hereinbelow, copies enclosed.

- (1) Japanese Patent Laid-Open No. 10-326949 (published on December 8, 1998). The abstract is attached hereto.
- (2) U.S. Patent No. 6,284,985 entitled CERAMIC CIRCUIT BOARD WITH A METAL PLATE..., By Naba et al., patented September 4, 2001. The patent is attached hereto.

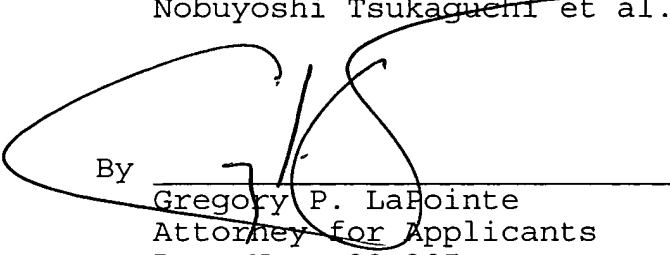
The undersigned submits the above-identified references for independent consideration by the Examiner and does not make any

admission that these references are or are not material to the present invention or that these references are or are not prior art with respect to the present invention.

Respectfully submitted,

Nobuyoshi Tsukaguchi et al.

By



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Date: January 19, 2004

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313" on January 19, 2004.



Rachel Piscitelli



Japanese Patent Laid-Open No. 10-326949 (published on December 8, 1998)

Japanese Patent Laid-Open No. 10-326949 discloses a circuit board comprising a ceramic substrate and a metal circuit which is bonded to the ceramic substrate via a bonding layer containing an active metal. The bonding layer containing the active metal protrudes from the bottom end portion of the metal circuit inside and/or outside to bond the metal circuit to the ceramic substrate. The shortest distance of the distances between metal circuits, between bonding layers and between the metal circuit and the bonding layer is in the range of from 0.5 mm to 1.0 mm. The length of the bonding layer protruding from the bottom end portion of the metal circuit is in the range of from  $-50\text{ }\mu\text{m}$  ( $50\text{ }\mu\text{m}$  inside) to  $+30\text{ }\mu\text{m}$  ( $30\text{ }\mu\text{m}$  outside), and the dimensional difference between the bottom and top end portions of the metal circuit is in the range of from  $50\text{ }\mu\text{m}$  to  $100\text{ }\mu\text{m}$ . This publication also discloses that the metal circuit has a thickness of between 0.3-0.5 mm and a skirt length of 50-100  $\mu\text{m}$ . Moreover, this publication discloses, in Comparative Example 1, a circuit board which has a metal circuit having a thickness of 0.3 mm and which a skirt length of 30  $\mu\text{m}$ .

US Patent No. 6,284,985 (issued on September 4, 2001)

US Patent No. 6,284,985 discloses a ceramic circuit board comprising: a ceramic substrate; a plurality of metal circuit plates bonded to a surface of the ceramic substrate; and parts including semiconductor element integrally bonded to a surface of the metal circuit plates through a solder layer, wherein at least peripheral portion of one metal circuit plate to which the parts are solder-bonded and which is adjacent to the other metal circuit plates is formed with a projection for preventing solder-flow. This patent also discloses that it is preferable for the direct bonding method to use metals which are liable to easily generate a eutectic compound from a component of the ceramic substrate.

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**Complete if Known**

Application Number	10/713,390
Filing Date	November 14, 2003
First Named Inventor	Nobuyoshi Tsukaguchi et al.
Group Art Unit	
Examiner Name	
Attorney Docket Number	02-668-CJP

(use as many sheets as necessary)

Sheet	1	of	1	Attorney Docket Number	02-668-CIP
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[illegible][illegible]Date  
Considered

<sup>1</sup> Unique citation designation number. <sup>2</sup> See attached Kinds of U.S. Patent Documents. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

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